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Acoustics, Speech, and Signal Processing, IEEE International Conference on ICASSP '87.

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Myjak, M.J.; Delgado-Frias, J.G.;

Circuits and Systems I: Regular Papers, IEEE Transactions on

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### A simple and ultra-fast DSP-based space vector PWM algorithm and its implementation on a two-level inverter covering undermodulation and overmodulation

Filho, N.P.; Pinto, J.O.P.; Borges da Silva, L.E.; Bose, B.K.;

Industrial Electronics Society, 2004. IECON 2004. 30th Annual Conference of IEEE

Volume: 2

Digital Object Identifier: [10.1109/IECON.2004.1431750](https://doi.org/10.1109/IECON.2004.1431750)

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### Implementation of a fixed-point MPEG-4 scalable lossless coding encoder

Choong Sang Cho; Yong-Hwan Kim; Hwa Seon Shin; Byeong Ho Choi;  
Broadband Multimedia Systems and Broadcasting (BMSB), 2010 IEEE International Symposium on  
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## An Optimized Design of Bit Plane Prediction Based Image Compression Algorithm on DSP

Zheng Zhao; Jiang Hongxue; Li Bo;  
Information Science and Engineering (ICISE), 2009 1st International Conference on  
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## Fast combinatorial RNS processors for DSP applications

Di Claudio, E.D.; Piazza, F.; Orlandi, G.;  
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## A universal nonlinear component and its application to WSI

Jain, V.K.; Wadekar, S.A.; Lei Lin;  
Components, Hybrids, and Manufacturing Technology, IEEE Transactions on  
 Volume: 16, Issue: 7  
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### Fault-tolerant serial-parallel multiplier

Chen, L.G.; Chen, T.H.;  
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### Improving Synthesis of Compressor Trees on FPGAs via Integer Linear Programming

Parandeh-Afshar, H.; Brisk, P.; Jenne, P.;  
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### Design of a Reed-Solomon decoder using a digital signal processor (DSP)

Todoroki, T.; Miura, S.;  
[Telecommunications Symposium, 1990. ITS '90 Symposium Record, SBT/IEEE International](#)  
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## A New Architecture for a SineWave Output DDS with High Spectral Purity

Kroupa, V.;

[Direct Digital Frequency Synthesizers](#)

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## A direct digital frequency synthesizer using an IIR filter implemented with a DSP microprocessor

Lo Presti, L.; Cardamone, G.;

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## An FPGA-specific algorithm for direct generation of multi-variate Gaussian random numbers

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[Application-specific Systems Architectures and Processors \(ASAP\), 2010 21st IEEE International Conference on](#)

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## Novel approach for implementing convolutions with small tables

Skavantzos, A.;

[Computers and Digital Techniques, IEE Proceedings E](#)

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Publication Year: 1991 , Page(s): 255 - 259

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### Fast Division on Fixed-Point DSP Processors Using Newton-Raphson Method

Nenadić, N.M.; Mladenović, S.B.;

[Computer as a Tool, 2005. EUROCON 2005. The International Conference on](#)

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### Improved multiplier of CSD used in digital signal processing

Lei Chen; Xiao-Yan Tian; Xiao-Jun Zhao;

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Meher, P.K.;

[VLSI System on Chip Conference \(VLSI-SoC\), 2010. 18th IEEE/ITP](#)Digital Object Identifier: [10.1109/VLSISOC.2010.5642660](#)

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### Low power DCT implementation approach for VLSI DSP processors

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### LUT Optimization for Memory-Based Computation

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## Parametric architecture for implementing multimedia algorithms

Kavvadias, N.; Nikolaidis, S.;

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## A flexible DSP block to enhance FPGA arithmetic performance

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### A reconfigurable Digital Signal Processor using residue number system

Banerjee, S.; Sinha, A.;

[Information Sciences Signal Processing and their Applications \(ISSPA\), 2010 10th International Conference on](#)  
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